



3.3V CMOS 1-TO-10 CLOCK DRIVER

IDT74FCT3807/A

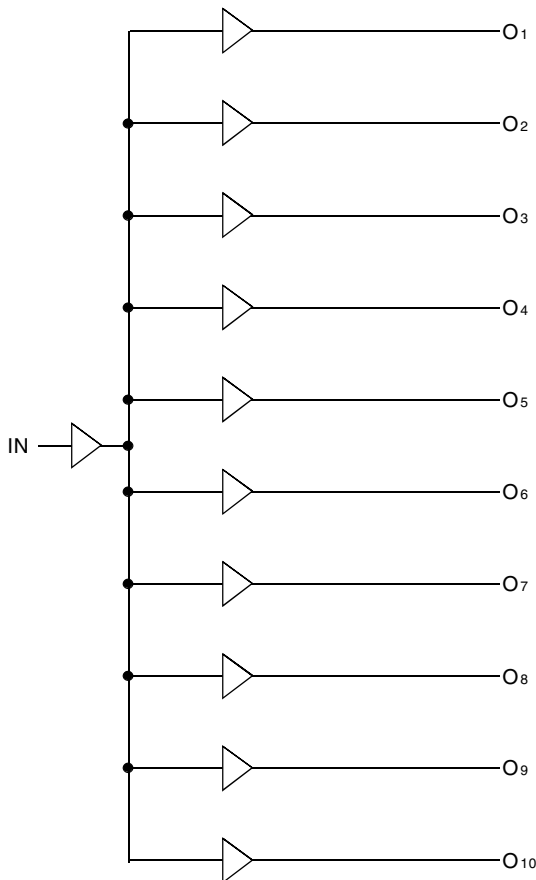
FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 350ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 3ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:10 fanout
- Maximum output rise and fall time < 1.5ns (max.)
- Low input capacitance: 4.5pF typical
- $V_{CC} = 3.3V \pm 0.3V$
- Inputs can be driven from 3.3V or 5V components
- Available in SSOP, SOIC, and QSOP packages

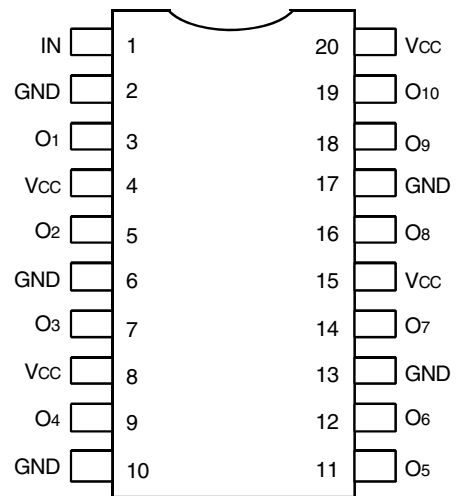
DESCRIPTION:

The FCT3807/A 3.3V clock driver is built using advanced dual metal CMOS technology. This low skew clock driver offers 1:10 fanout. The large fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. The FCT3807/A offers low capacitance inputs with hysteresis for improved noise margins. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +60	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
IN	Clock Inputs
Ox	Clock Outputs

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = V _{CC} - 0.6V ⁽³⁾	—	10	30	μA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Input toggling 50% Duty Cycle Outputs Open	V _{IN} = V _{CC} V _{IN} = GND	—	0.31	0.45 mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Input toggling 50% Duty Cycle Outputs Open f _i = 50MHz	V _{IN} = V _{CC} V _{IN} = GND	—	15.5	22.8 mA
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	15.5	22.8

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input (V_{IN} = V_{CC} - 0.6V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_i)
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} - 0.6V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Input Frequency
 All currents are in milliamps and all frequencies are in megahertz.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Commercial: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Unit	
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	5.5	V	
	Input HIGH Level (I/O pins)		2	—	$V_{CC} + 0.5$		
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedence Output Current (3-State Output Pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V	
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$	-36	-60	-110	mA	
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$	50	90	200	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	—	V
			$I_{OH} = -8\text{mA}$	$2.4^{(5)}$	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.5	
I_{OFF}	Input Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} = 4.5\text{V}$	—	—	± 1	μA	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	-60	-135	-240	mA	
V_H	Input Hysteresis	—	—	150	—	mV	
I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC}	—	0.1	10	μA	
I_{CCH}			—	—	—		
I_{CCZ}			—	—	—		

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}, +25^{\circ}\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL^(3,4)

Symbol	Parameter	Conditions ⁽¹⁾	FCT3807		FCT3807A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	50Ω to V _{CC} /2 C _L = 10pF	1.5	3.5	1.5	3	ns
t _R	Output Rise Time	(See figure 1)	—	1.5	—	1.5	ns
t _F	Output Fall Time	or 10Ω AC termination,	—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of same package (same transition)	C _L = 50pF	—	0.5	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})	(See figure 2) f ≤ 100MHz	—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	Outputs connected in groups of two	—	0.9	—	0.65	ns

Symbol	Parameter	Conditions ⁽¹⁾	FCT3807		FCT3807A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 30pF f ≤ 67MHz	1.5	4.5	1.5	4	ns
t _R	Output Rise Time	(See figure 3)	—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of same package (same transition)		—	0.5	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1	—	0.75	ns

Symbol	Parameter	Conditions ⁽¹⁾	FCT3807		FCT3807A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 50pF f ≤ 40MHz	1.5	4.8	1.5	4.3	ns
t _R	Output Rise Time	(See figure 4)	—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of same package (same transition)		—	0.5	—	0.35	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.5	—	0.35	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1	—	0.75	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL (3,4)

Symbol	Parameter	Conditions ⁽¹⁾	FCT3807		FCT3807A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	50Ω to V _{CC} /2 C _L = 10pF	1.5	3.5	1.5	3	ns
t _R	Output Rise Time	(See figure 1)	—	1.5	—	1.5	ns
t _F	Output Fall Time	or 50Ω AC termination,	—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of same package (same transition)	C _L = 10pF	—	0.6	—	0.45	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})	(See figure 2) f ≤ 100MHz	—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	Outputs connected in groups of two	—	0.9	—	0.65	ns

Symbol	Parameter	Conditions ⁽¹⁾	FCT3807		FCT3807A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 30pF f ≤ 67MHz	1.5	4.5	1.5	4	ns
t _R	Output Rise Time	(See figure 3)	—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of same package (same transition)		—	0.6	—	0.45	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1	—	0.75	ns

Symbol	Parameter	Conditions ⁽¹⁾	FCT3807		FCT3807A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay	C _L = 50pF f ≤ 40MHz	1.5	4.8	1.5	4.3	ns
t _R	Output Rise Time	(See figure 4)	—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
tsk(O)	Output skew: skew between outputs of same package (same transition)		—	0.6	—	0.45	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	0.6	—	0.45	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1	—	0.75	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS

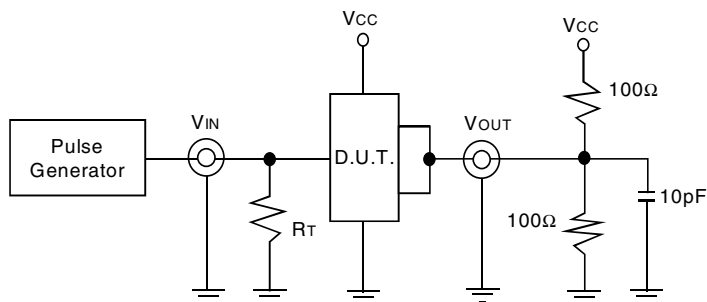


Figure 1. $Z_o = 50\Omega$ to $V_{cc}/2$, $C_L = 10pF$

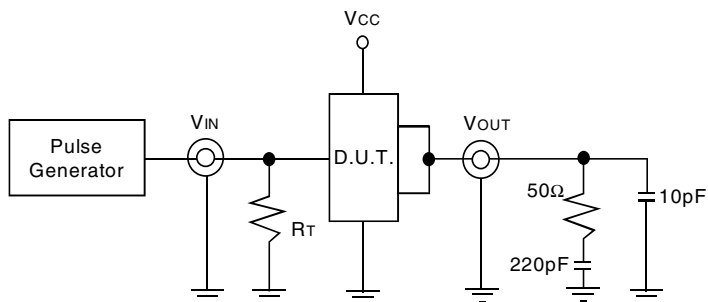


Figure 2. $Z_o = 50\Omega$ AC Termination, $C_L = 10pF$

The capacitor value for ac termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

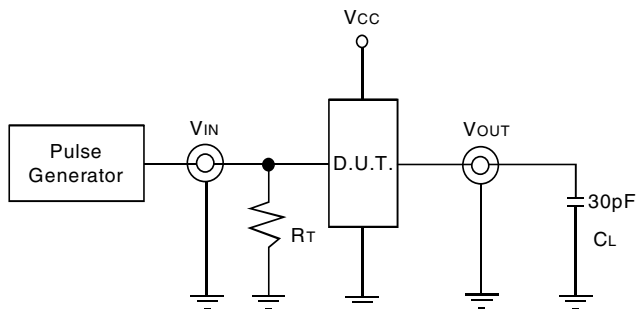


Figure 3. $C_L = 30pF$ Circuit

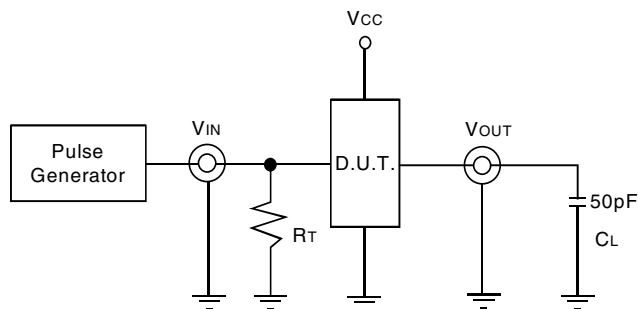


Figure 3. $C_L = 50pF$ Circuit

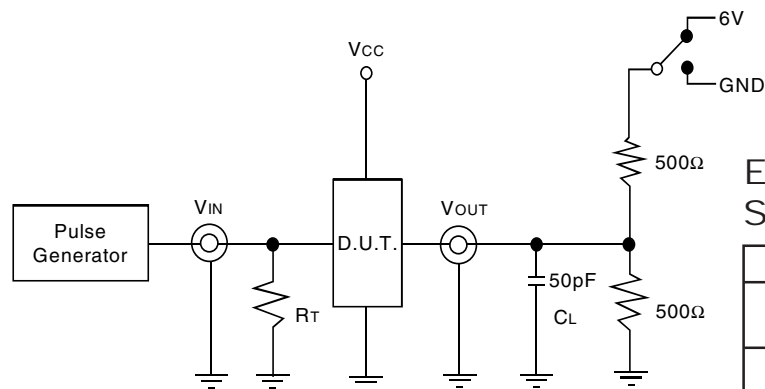


Figure 5. Enable and Disable Time Circuit

ENABLE AND DISABLE TIME SWITCH POSITION

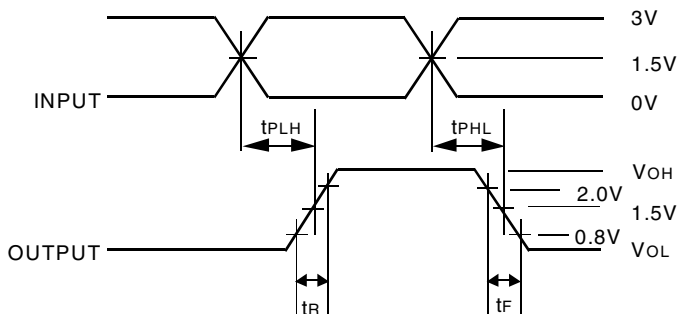
Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND

DEFINITIONS:

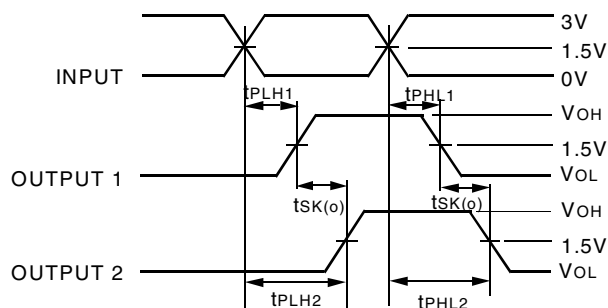
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

TEST WAVEFORMS

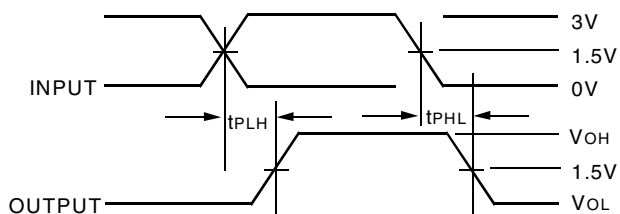


Package Delay



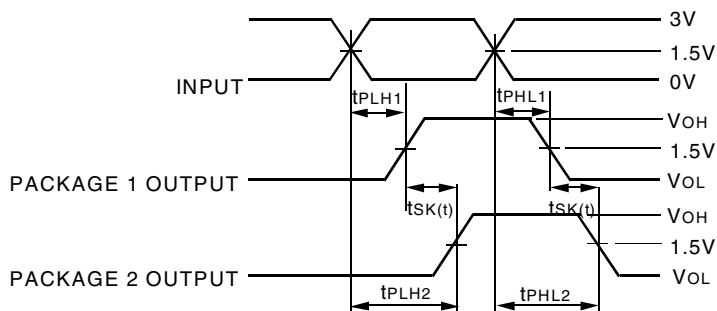
$$t_{SK(O)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew - $t_{SK(O)}$



$$t_{SK(P)} = |t_{PHL} - t_{PLH}|$$

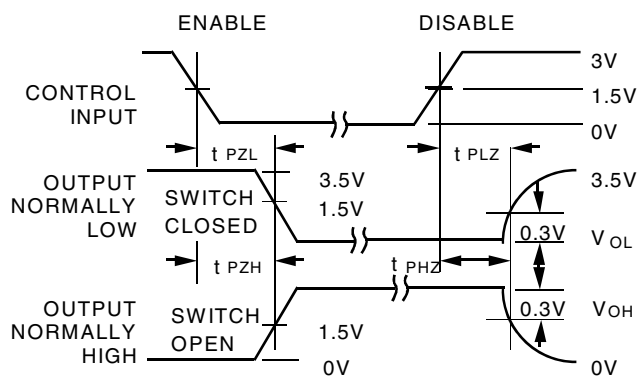
Pulse Skew - $t_{SK(P)}$



$$t_{SK(T)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Package Skew - $t_{SK(T)}$

Package 1 and Package 2 are same device type and speed grade

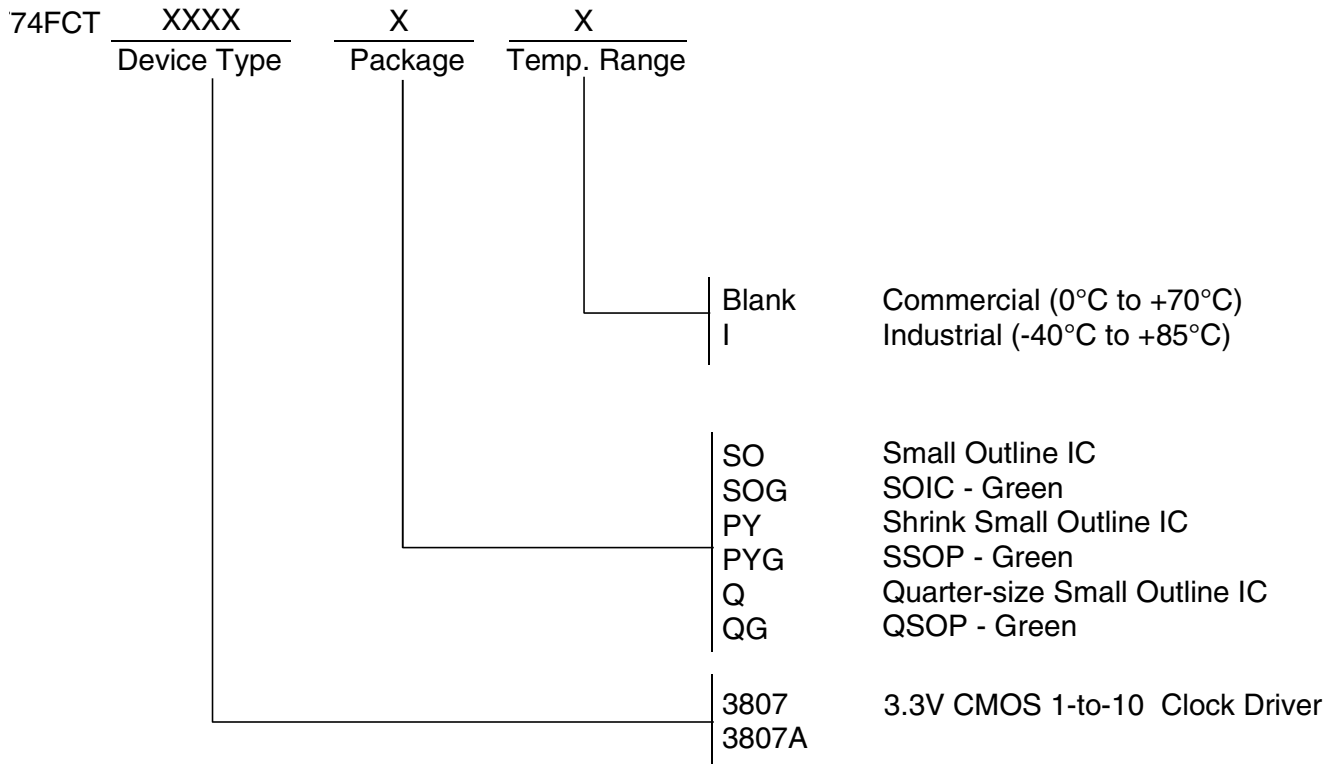


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION



CORPORATE HEADQUARTERS
 6024 Silver Creek Valley Road
 San Jose, CA 95138

for SALES:
 800-345-7015 or 408-284-8200
 fax: 408-284-2775
 www.idt.com

for Tech Support:
 clockhelp@idt.com